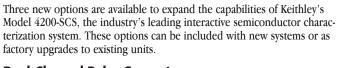
## Pulse and Pulse I-V Options for the Model 4200-SCS

## Technical Data Sheet Addendum



## **Dual-Channel Pulse Generator**

The Model 4200-PG2 Dual-Channel Pulse Generator integrates pulsing with the Model 4200-SCS's DC source and measure capabilities. It provides voltage pulses as short as 20ns in high speed mode or up to  $\pm 20V$  (into  $50\Omega$ ) in high voltage mode. Adding the 4200-PG2 to the Model 4200-SCS expands the system's range of applications significantly, including:

- Charge pumping for interface charge trap characterization
- AC stress for stress/measure reliability testing
- Basic clock generation for test vectoring and failure analysis
- Digital triggering for multi-pin device testing

Using a supplied User Test Module (UTM), it's simple to incorporate pulse generation

into KITE test sequences. The pulse generator can also be driven as a stand-alone pulser for maximum flexibility and ease of use with the supplied Graphical User Interface (GUI). Support is provided for controlling a wide range of operating variables, including pulse frequency, duty cycle, rise/fall time, amplitude, and offset, as well as the ability to trigger single pulses and/or pulse trains.



## **Digital Oscilloscope**

The Model 4200-SCP2 Oscilloscope offers both general purpose scope capabilities and time-domain measurements to complement the pulser's time-domain sourcing. The scope can be programmed for automated measurement and data acquisition or used with the standalone GUI application provided to perform traditional oscilloscope tasks. The scope makes measurements in both the time (frequency, rise/fall time) and voltage domains (amplitude, peak-peak, etc.) The measurements can be applied to the entire captured waveform or a selected portion of the waveform by setting cursors.

## Pulse I-V Package

The Pulse I-V package combines the PG2 dual-channel pulse generator, the SCP2 oscilloscope, the specialized interconnect, and patent-pending software to provide a turnkey pulse I-V solution. The software controls sourcing from the pulse generator and data acquisition to automate a variety of pulse I-V tests. The Model 4200's proven interface handles instrument setup and control, as well as data storage and presentation. The innovative software provides both cable compensation and load-line compensation, producing DC-like I-V transistor curves, such as  $V_{\rm DS}\text{-}I_{\rm D}$  family of curves and  $V_{\rm GS}\text{-}I_{\rm D}$  for voltage threshold extraction. This solution provides pulse I-V testing for devices with self-heating issues, such as high power transistors and advanced CMOS on SOI technology. The Pulse I-V package includes sample projects to address the charge trapping problems for high  $\kappa$  gate structures. The specialized interconnect solves most of the problems encountered in high speed pulse testing, such as:

- Combining pulse and DC sources to a single DUT pin to permit both DC and pulse characterization without any re-cabling or switching
- Impedance matching to minimize reflection and maintain pulse fidelity
- Straightforward cabling and connection to DUT provides easy setup

The Pulse I-V package provides the user with an easy-to-understand solution right out of the box, while offering access to the pulse generator and scope for general purpose pulse and scope applications.



- Dual-channel pulse generator and scope cards (4200-PG2 and 4200-SCP2) support both pulsed I-V testing for devices with selfheating issues and general purpose pulsing and pulse measurement\*
- The 4200-PIV package provides a complete pulse I-V solution for the powerful Model 4200-SCS platform\*
  - Includes pulse and scope cards
  - Pulse I-V software included provides both cable compensation and load-line compensation
  - Specialized interconnect designed specifically for high speed pulse testing
  - \* Option for either new or existing Model 4200-SCS systems

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## Ordering Information\*\*

### 4200-PIV

Pulse I-V Option for the Model 4200-SCS (includes 4200-PG2, 4200-SCP2, Software, and Specialized Interconnect Hardware

## 4200-PG2

**Dual-Channel Pulse Generator Card** 

#### 4200-SCP2

Dual-Channel Oscilloscope Card

## 4200-SCP2-ACC Optional Scope Probe

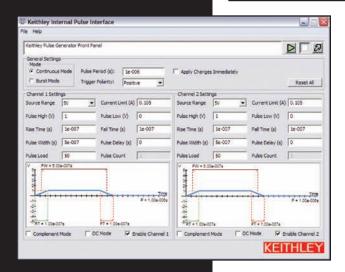
## Pulse and Pulse I-V Options for the Model 4200-SCS

Technical Data Sheet Addendum

## 4200-PG2 Specifications1

| PULSE/LEVEL <sup>2</sup>    |                                     |   |   |
|-----------------------------|-------------------------------------|---|---|
|                             |                                     | HIGH SPEED  | HIGH VOLTAGE                                      |
| AMPLITUDE                   | 50 Ω into 50 Ω                      | 100 mV p-p to 10 V p-p                            | 500 mV p-p to 40 V p-p                            |
|                             | 50 $\Omega$ into 1 $\text{M}\Omega$ | 200 mV p-p to 20 V p-p                            | 1 V p-p to 80 V p-p                               |
| DC LEVEL                    |                                     | -5.0 V to +5.0 V                                  | -20.0 V to +20.0 V                                |
|                             | Accuracy                            | $\pm (3\% + 50 \text{ mV})$                       | $\pm (3\% + 100 \text{ mV})$                      |
| AMPLITUDE/LEVEL             | 50 $\Omega$ into 50 $\Omega$        | 1 mV  | 5 mV  |
| RESOLUTION                  | 50 $\Omega$ into 1 $\text{M}\Omega$ | 2 mV  | 10 mV   |
| OUTPUT CONNECTORS           |                                     | SMA   | SMA   |
| SOURCE IMPEDANCE            |                                     | 50 $\Omega$ nominal                               | 50 Ω nominal                                      |
|                             | Accuracy                            | ±0.5%   | ±0.5%   |
| SHORT CIRCUIT CURRENT       |                                     | ±200 mA   | ±800 mA peak                                      |
| BASELINE NOISE              |                                     | $\pm (0.1 \% + 5 \text{ mV}) \text{ RMS typical}$ | $\pm (0.1 \% + 5 \text{ mV}) \text{ RMS typical}$ |
| OVERSHOOT/PRE-SHOOT/RINGING |                                     | ±5% of amplitude ±20 mV                           | ±5% of amplitude ±80 mV                           |
| OUTPUT LIMIT                |                                     | Programmable limit to protect the DUT             |   |

| TIMING                            |            |  |  |  |
|-----------------------------------|------------|--|--|--|
|                                   |            | HIGH SPEED   | HIGH VOLTAGE                                 |  |
| FREQUENCY RANGE                   |            | 1 Hz to 50 MHz   | 1 Hz to 2 MHz                                |  |
| TIMING RESOLUTION                 |            | 10 ns  | 10 ns  |  |
| RMS JITTER (period, width)        |            | 0.01 % + 200 ps typical  |  |  |
| PERIOD RANGE                      |            | 20 ns to 1s (See Figure 1.)  | 500 ns to 1 s                                |  |
|                                   | Accuracy   | ±1%  | ±1%  |  |
| PULSE WIDTH RANGE                 |            | 10 ns to (period – 10 ns)  | 250 ns to (period – 100 ns)                  |  |
|                                   | Accuracy   | $\pm (3\% + 200 \text{ ps})$   | $\pm (3\% + 5 \text{ ns})$                   |  |
| PROGRAMMABLE<br>TRANSITION TIME   | (0 – 100%) | 10 ns − 1 s  | 100 ns − 1 s                                 |  |
| TRANSITION SLEW RATE <sup>3</sup> | Accuracy   | ±1% for transition time ≥100 ns  | $\pm 1\%$ for transition time $\geq 1 \mu s$ |  |
|                                   | Linearity  | 3% for transition time ≥100 ns   | 3% for transition time ≥500 ns               |  |
| TYPICAL MIN. TRANSITION           |            | < 15 ns  | < 150 ns                                     |  |
| TIME (10-90%)                     |            | Pulse period and width are variable in 10ns steps without any output glitches or dropouts. |  |  |



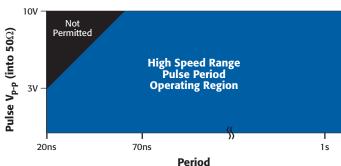


Figure 1. Permitted area of operation.

Pulse interface GUI for general purpose pulse operations.

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<sup>\*\*</sup> Adding any of these options to an existing Model 4200-SCS system requires upgrading to the most current version of the hardware (Pentium 4 CPU or 4200-CPU-2GH) and software (V. 6.0). Contact your sales engineer or the factory for details on these upgrade requirements.

## Pulse and Pulse I-V Options for the Model 4200-SCS

Technical Data Sheet Addendum

## **4200-SCP2 Specifications**

### **ANALOG INPUT<sup>4</sup>**

CHANNELS QUANTITY: 2.

**BANDWIDTH** (50 $\Omega$ ): DC to 1GHz.

**BANDWIDTH** (1M $\Omega$ ): DC to 500MHz.

MAXIMUM INPUT (50 $\Omega$ ):  $\pm 5$ VDC, input load protection @  $\pm 6$ VDC.

MAXIMUM INPUT (1M $\Omega$ ):  $\pm 150$  DC, derated 20dB/decade above 1MHz.

**FULL SCALE INPUT RANGE (50\Omega):** 0.05, 0.1, 0.25, 0.5, 1, 2, 5, 10 (Vp-p).

FULL SCALE INPUT RANGE (1M $\Omega$ ): 0.1, 0.2, 0.5, 1, 2.5, 5, 10, 20, 50, 100 (Vp-p).

DC GAIN ACCURACY: <±1% of full scale.

IMPEDANCE:  $1M\Omega \mid \mid 12pF$  or  $50\Omega$ 

IMPEDANCE ACCURACY:  $\pm 1\%$ .

COUPLING: DC or AC.

OFFSET ADJUST: ±(full scale range/2).

OFFSET ACCURACY: ±(1% offset + 1% full scale).

INPUT CONNECTOR: BNC.

### **ANALOG-TO-DIGITAL CONVERTER**

RESOLUTION: 8-bit.

SAMPLE RATE: 2.5kS/s to 1.25GS/s in 1, 2.5, 5 steps. 2.5GS/s (1 channel interleaved).

ACQUISITION TIME RANGE: 50ns to 419 seconds.

ACQUISITION MODES: Normal, Average, Envelope, and Equivalent-Time.

#### **TRIGGER**

TRIGGER SOURCE: Channels 1 to 2, External, Pattern, Software.

POST-TRIGGER DELAY: 0 to 655 seconds.

 $\label{eq:pre-trigger} \textbf{PRE-TRIGGER DELAY:} \ 0 \ to \ waveform \ time.$ 

TRIGGER HOLD OFF RANGE: 0 to 655 seconds.

TRIGGER MODES: Edge or Pulse Width.

EDGE TRIGGER MODE: Rising or Falling Edge.

PULSE WIDTH RANGE: 20ns to 655 seconds, 10ns resolution.

EXTERNAL TRIGGER INPUT: TTL compatible,  $10k\Omega$  input impedance.

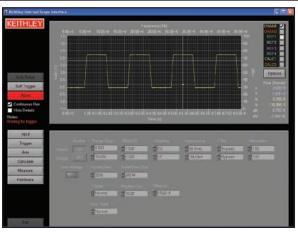
CONNECTOR: SMB.

## **OPTIONAL SCOPE PROBE: 4200-SCP2-ACC**

 BANDWIDTH: 500MHz.
 ATTENUATION:  $10\Omega$  fixed.

 MAX. DC: 600V DC rated.
 LOADING: 8pF and  $10M\Omega$ .

 LENGTH: 1 meter.
 CONNECTOR: BNC.



Scope interface GUI for general purpose scope operations.



Optional scope probe (4200-SCP2-ACC).

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# Pulse and Pulse I-V Options for the Model 4200-SCS

## Technical Data Sheet Addendum

## 4200-PIV Typical Specifications<sup>1</sup>

CHANNELS: 2.

TYPICAL PULSE PERFORMANCE:

| Measurement          | With 4200 Remote Bias Tee<br>(Figure 2)             | Without 4200 Remote Bias<br>Tee (Figure 3)            |
|----------------------|---|---|
| Accuracy             | <4% of signal ±1mV <sup>6</sup>                     | N/A   |
| Max. Current         | 100 mA @ PW = 40–150 ns                             | 100  mA @ PW = 40  ns                                 |
| Resolution           | Maximum $5\mu$ A, $250\mu$ V<br>8-bit A/D converter | Maximum $5\mu$ A, $250\mu$ V<br>8-bit A/D converter   |
| Sample Rate          | 1.25 Gsample/s                                      | 1.25 Gsample/s  |
| Duty Cycle           | <0.1%   | <0.1%   |
| DC Offset            | ±200 V  | N/A   |
| Min. Transition Time | 10 ns <sup>7</sup>                                  | See PG2 specs   |
| Maximum V            | $10 \text{ Vpp into } 50\Omega^7$                   | $10 V_{\rm pp}$ into gate, $40 V_{\rm pp}$ into drain |
| Max. Pulse Width     | 150 ns  | See PG2 specs   |

SMU TYPICAL DC PERFORMANCE (with 4200 Remote Bias Tee):

Leakage: 1–10nA/V<sup>5</sup>. Noise: 1–10nA RMS.

Max. Voltage: 200V (>40V requires safety interlock and related precautions).

Max. Current: 0.5A.

4200 REMOTE BIAS TEE TYPICAL PERFORMANCE:

Band Pass: 10kHz-300MHz (3dB).

Power Divider Max. Power Input: 0.125W DC.

#### **NOTES**

- 1 Unless stated otherwise, all specifications assume a  $50\Omega$  termination.
- 2 Level specs are valid after 50ns typical settling time (after slewing) for the high speed mode and after 500ns typical settling time (after slewing) for the high voltage mode into a  $50\Omega$  load.
- 3 Specs apply to a 10–90% transition, typical.
- 4 Inputs are referenced to 4200 chassis ground.
- 5 Leakage measured after a five-second settling time.
- 6 All typical specs apply to the AC+DC output connector of the 4200 Remote Bias Tee interconnect box and after system compensation.
- 7 4200 Remote Bias Tee supports the 4200-PG2 high speed range only.

All specifications apply at 23° ±5°C, within 1 year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

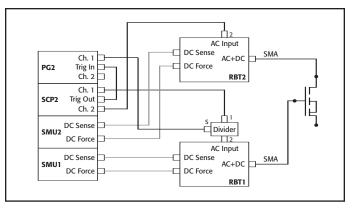


Figure 2. Interconnect for pulse I-V (high  $\kappa$  charge trapping and isothermal testing).

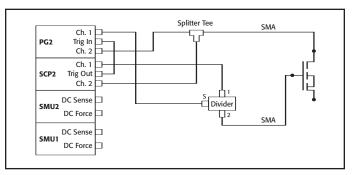


Figure 3. Interconnect for single pulse charge trapping.

Specifications are subject to change without notice. Refer to **www.keithley.com** for the latest product information.

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